Amendments to the Claims:

1. (Currently Amended) A **single** computer system comprising:

a central processing unit;

a plurality of peripheral devices operatively associated with said central processing unit **within said single computer system** and comprising volatile memory, non-volatile memory, and a plurality of I/O subsystems to and from which data flows are exchanged with said central processor for processing of data by said central processing unit; and

a network processor operatively interposed between said central processing unit and said peripheral devices and among said peripheral devices, said network processor having

a plurality of interface processors;

instruction memory storing instructions accessibly to said interface processors;

data memory storing accessibly to said interface processors data passing through said network processor from and to said peripheral devices; and

a plurality of input/output ports exchanging data passing through said network processor with said peripheral devices;

said network processor cooperating with said central processing unit in directing the exchange of data between said input/output ports and the flow of data through said data memory to and from said volatile memory and said non-volatile memory in response to execution by said interface processors of instructions loaded into said instruction memory.

2. (Original) Apparatus according to Claim 1 wherein said network processor comprises a semiconductor substrate and further wherein said interface processors, said instruction memory, said data memory and said input/output ports are formed on said semiconductor substrate.

3. (Original) Apparatus according to Claim 1 wherein the number of said interface processors exceeds four.

4. (Original) Apparatus according to Claim 1 wherein one of said input/output ports is operatively connected with each corresponding one of said plurality of I/O subsystems.